REMARKS

I. Introduction

At the time of the Office Action dated May 12, 2006, claims 1-13 are pending in this application. In this Amendment, claims 1, 8, 12 and 13 have been amended, and new claims 14-16 have been added. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the amendment can be found in, for example, Fig. 1 and relevant description of the specification. Now, claims 1-16 are active in this application, of which claims 1, 8, 12 and 13 are independent.

II. Information Disclosure Statement

An Information Disclosure Statement was filed on July 20, 2006. Applicants respectfully request the Examiner to acknowledge receipt of the IDS and provide a copy of the PTO-1449 form appropriately initialed indicating consideration of the cited references.

III. The Rejection of Claims 1-13

Claims 1-13 have been rejected under 35 U.S.C. §102(b) as being anticipated by Ellis.

The Examiner asserted that Ellis discloses an application specific automated test equipment system for testing integrated circuit devices in a native environment, identically corresponding to what is claimed.

In more detail, Ellis discloses ATE (Automated Test Equipment) system 200 which includes application specific ATE unit 202 connected to control computer 204 as shown in Fig. 2. In the system, device under the test (DUT) 208 is mounted on native interface board 206.

ATE unit 202 executes test routines, and a test signal is sent to DUT 208 through native interface

board 206. For example, resident devices and resident clock unit 313 providing a resident clock signal to each of the resident devices are mounted on the native interface board (see Fig. 3A).

Applicants submit that Ellis does not disclose an assembly for an LSI test including all the limitations recited in independent claim 1, as amended. Specifically, the reference does not disclose, at a minimum, the following limitations:

a peripheral circuit coupled to the target LSI and allowing the target LSI to operate in the same manner as in actual operation;

a plurality of clock generators to generate clocks asynchronous with each other and to supply the clocks to the target LSI; and

a printed circuit board on which the peripheral circuit and the plurality of clock generators are mounted.

The assembly for an LSI test in claim 1 includes a peripheral circuit coupled to a target LSI and a plurality of clock generators for generating clocks asynchronous with each other and supplying the clocks to the target LSI. These elements enable the target LSI to operate in the same manner as in actual operation. It is, therefore, possible to test a system LSI having a feature such as asynchronous operation between input/output of data and internal operation, or multiple clocks.

The native interface board of Ellis embodies or recreates a native environment of the device under test. Resident devices and the resident clock unit are mounted on the native interface board. The resident clock unit on the interface board merely provides a resident clock signal to each of the resident devices on the interface board (column 6, lines 5-7).

Application No.: 10/637,663

In the claimed invention, the peripheral circuit and the plurality of clock generators are mounted on a printed circuit. However, the plurality of clock generators are configured for supplying asynchronous clocks to the target LSI, but not to the peripheral circuit on the printed circuit.

Accordingly, Ellis does not identically disclose an assembly for an LSI including all the limitations recited in independent claim 1, as amended. The above discussion is applicable to independent claims 8, 12 and 13. Dependent claims are also patentably distinguishable over Ellis at least because the claims respectively include all the limitations recited in independent claims 1 and 8. Applicants, therefore, respectfully solicit withdrawal of the rejection of claims 1-13 under 35 U.S.C. §102(b) and favorable consideration thereof.

IV. New Claims 14-16

Applicants submit that new claims 14-16 are patentably distinguishable over Ellis at least because the claims respectively include all the limitations recited in independent claims 1, 8 and 12, and solicit favorable consideration thereof.

V. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

Application No.: 10/637,663

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Please recognize our Customer No. 20277

as our correspondence address.

Michael Eurogarty
Registration No. 36.13

600 13th Street, N.W. Washington, DC 20005-3096 Phone: 202.756.8000 MEF:TT/cac

Facsimile: 202.756.8087 **Date: August 14, 2006**

WDC99 1269786-1.060188.0632